METHOD AND APPARATUS FOR MANAGING THE CONFIGURATION AND FUNCTIONALITY OF A SEMICONDUCTOR DESIGN

The present application claims priority to U.S. Provisional Patent Application Serial Number 60/104,271, entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design" filed October 14, 1998.

Copyright

1. Field of the Invention

The invention relates generally to the field of semiconductor design and layout and computer automated design (CAD) for semiconductors. More specifically, the invention provides a method for managing the configuration, design parameters, and functionality of an integrated circuit design in which custom instructions and other elements may be arbitrarily controlled by the designer.

2. Description of Related Technology

Several types of computer aided design (CAD) tools are available to design and fabricate integrated circuits (IC). Such computer-aided or automated IC design tools can include modules or programs addressing both the synthesis and optimization processes. Synthesis is generally defined as an automatic method of converting a higher level of abstraction to a lower level of abstraction, and can include any desired combination of synthesis techniques which occur at various levels of abstraction. So-called "behavioral synthesis" is a design tool wherein the behavior (e.g. inputs, outputs, and functionality) of a desired IC are entered into a computer program to design a device that exhibits the desired behavior. Such tools permit IC designers to produce increasingly complex and capable devices, sometimes having logic gate counts in the

APPENDIX I

The following describes and illustrates the operation of the ARC System Builder Program:

Installation Script

Installation script allowing the following ARC features to be selected:

- ?Extensions required
- ?Cache size
- ?Cache line length
- ?Size of external memory space that is to be cached.
- ?Clock period
- ?Clock skew
- ?Synthesized d-latches or 3-port RAM for register file
- ?Type of technology being used.
- ?Manufacturer code and version number information
-

The script creates a working directory for the user, and in it creates the following:

- VHDL for the extensions selected
- VHDL for a direct mapped I-cache configured to user's specification
- VHDL test-bench for testing basecase operation and external interfaces
- VHDL structure to link together all required modules
- Configuration files for Synopsys Design Compiler
- Memory image file containing basecase test code
- Synthesis script for Synopsys Design Compiler v3.4b or above
- Makefile - set up for the Model Technologies VSystem/VHDL simulator, but can be altered for use with other simulation environments.

The user can select from 4 different types of build:

- Core Build
- Generic System Build
- Altera Build (for ARCAngel™ development board)
- Core Verification System

After setting up his ARC area, before the user can use the *ARC system builder,* several environment variables need to be set.

In .cshrc:

Set ARCHOME environment variable, base of the arc install tree. Add bin directories to path. Set other environment variables such as ARC_MANCODE and ARC_MANVER and ARCASIC. (If these variables are not set the build script will ask for them at run time.)

e.g.

setenv ARCHOME /apps/ARC Cores

APPENDIX II

List of Script files

system_builder	
anARChy.awk	The main script. Called by system_builder
arc_mti_inst	Installation for ModelTech VHDL simulator
xentity	
entity.awk	Extract inputs + outputs from a VHDL file.
extant	Does a file exist already?
header.vhdl	VHDL header. Used by vhdlgen.awk.
hiergen	Generate a hierarchy. Calls vhdlgen.
hiergen.awk	called by makefile (makegen)
make_arc_sys_struct	Specific script for generating a hierarchy.
makegen	Generate makefile for building hierarchy
makegen.awk	calls hiergen, vhdlgen etc.
mti_make	Generate VHDL compilation makefiles
mti_make.awk	
synopsys_make	Generates Synopsys synthesis scripts
synopsys_make.awk	
up_xent	Update entity datafile. (makegen makefile).
vhdlcopy	Copies generated VHDL to user's vhdl/ dir
vhdlgen	Generate a structural vhdl file based on a hierarchy definition.
vhdlgen.awk	
vhdlmerge.awk	Merge extension data into a placeholder.
dat/apex.hier	Sample hierarchy file. (Ignore %%..%% keywords)
dat/apex.mg	Control file for hierarchy builder
dat/library.list	Sample library definition file.
sample/placeholder/xalu.vhdl	
sample/placeholder/xaux_regs.vhdl	Standard ARC extension placeholder files. Note -- ARCPRAGMA's
sample/placeholder/xcoreregs.vhdl	
sample/placeholder/xrctl.vhdl	
sample/extension/xalu.vhdl	Extension files for SWAP instr.
sample/extension/xrctl.vhdl	Merged into placeholders.